REMARKS

Claims 1-14 and 31-32 are pending in the application with the present amendments. Claims 15-30, which were not elected in response to the restriction requirement, are cancelled herein.

Applicants appreciate the early indication of allowability in the Office Action as to claims 6 and 7. Claims 1-5 and 8-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,126,636 to Wu ("*Wu*") in view of U.S. Patent No. 6,891,192 to Chen et al. ("*Chen*"). Claim 14 was rejected under 35 U.S.C. §102(e) as being anticipated by *Chen*. For the reasons set forth below, applicants respectfully request reconsideration and withdrawal of the rejections.

As amended herein, independent claim 1 recites a field effect transistor ("FET") having a pair of regions consisting essentially of a single-crystal semiconductor alloy. Each of the semiconductor alloy regions is spaced a first distance from the gate of the FET. Claim 1 further recites that the source region and the drain region of the FET are each spaced a second distance from the gate, the second distance being different from and independent from the first distance. The second distance is at least partly determined by spacings of first spacers from sidewalls of the gate.

Applicants respectfully submit that the combined teachings of *Wu* and *Chen* neither teach nor suggest these features recited in claim 1. *Wu* merely shows an FET in which *salicide* regions 30 are disposed at locations outward from spacers 26 (See col. 5, ln. 63 through col. 6, ln. 17). However, the distinction recited in claim 1 is that the *source*

and drain regions of the FET are spaced a second distance from the gate, the second distance being different and independent from a first distance at which the *semiconductor alloy regions* are spaced.

The portions of *Chen* cited by the Examiner do not provide the teachings which *Wu* lacks. While the source-drain regions 11 of the PFET 10 (FIG. 1) in *Chen* are "displaced from the gate conductor 26" by spacers 29 and 30 (col. 3, lns. 22-25), the semiconductor alloy regions 21 appear to be within the same trench as the source-drain regions 11. The source-drain regions 11 do not appear to be spaced from the gate of PFET 10 at a different distance than the semiconductor alloy regions 21.

Claim 14 contains similar recitations and is believed to be patentable in relation to *Wu* and *Chen* for at least the same reasons as provided above.

Support for the present amendments is provided, *inter alia*, at paragraphs **[0013]** and **[0021]** and **[0033]** of the Specification.

It is believed that no fees are required upon filing this Amendment. However, if any fees are required, authorization is given to debit the Deposit Account No. 09-0458 of the Assignee International Business Machines Corporation. If there is an overpayment, please credit the same account.

Respectfully submitted,
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By: _____

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